

FPGA Implementation of Binary Quasi Cyclic LDPC Code with Rate 2/5

Arulmozhi M.¹, Nandini G. Iyer², Anitha M.³

Assistant Professor, Department of EEE, Rajalakshmi Engineering College, Chennai, India¹

Assistant Professor, Department of EEE, Rajalakshmi Engineering College, Chennai, India²

Technical Associate, Tata Communications Limited, India³

ABSTRACT: LDPC (Low Density Parity Check) is a linear block code that has become one of the most attractive error correction codes due to its excellent performance and suitability in high data rate applications. These codes are specified in terms of parity check matrix (PCM) which is characterized by its sparsity. This PCM can be constructed either randomly or with structured pattern. This paper presents an overview of different PCM construction algorithms (both random and structured), software implementation of the LDPC decoder using MATLAB, and discusses about the LDPC decoder VLSI implementation using the commercial FPGA, Spartan 3E kit. The main focus is the nominal comparison between Quasi cyclic LDPC and Random LDPC in terms of area. This quasi cyclic decoder not only significantly reduces the computational complexity due to sparseness, but also the area, in comparison with random PCM.

KEYWORDS: Low Density Parity Check (LDPC), Parity Check Matrix (PCM), Sum Product Algorithm (SPA).

I. INTRODUCTION

In recent years, one of the most challenging issues in a communication system is to send zero-error data from the sender to receiver, in order to retain the originality of data. To improve the communication system which should have error free communication Shannon proposed the creative algorithm in 1948. By using Shannon's algorithm the data was changed and transmitted without error. After that, many innovative coding techniques have been invented and implemented. Several error coding techniques have been developed in order to encode and decode the transmitted data such as convolution code, Reed Solomon, turbo code and BCH to name a few.

In the early 1960's Gallager first introduced low-density parity check (LDPC) block codes. He also proposed an iterative decoding algorithm, which could achieve low error probabilities at high data rates, at a reasonable cost.

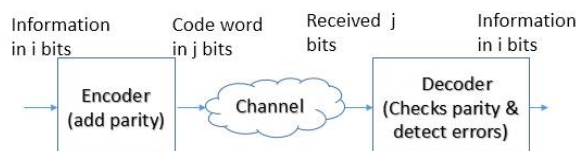


Fig. 1 Encoding-decoding system

Figure 1 shows encoding and decoding methodology of an 'i' bits communication system. The 'i' bits of original information is encoded in the transmitter block, which adds the parity and gives the j bits of modified data as a code word. The received j bits code word through the channel can be decoded to check parity and detect error.

The original 'i' bits are retrieved in decoding block without errors. The cyclic codes given by PCM in the circulant form can be decomposed into descendant quasi-cyclic codes of different lengths and rates using column-row permutations. Codes in these classes have low error-floors. Alberto J.F *et.al*, discuss how convolutional codes

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outperform block codes of the same length and a small inter-leaver size low density convolutional codes are superior to turbo codes [1]. Continuous decoding process for LDPC codes was described. Time varying and time –invariant LDPC convolution codes with low encoding and decoding complexities can be derived from block codes .LDPC convolution code can achieve good performance with low encoding and decoding complexity[2]. The performance of Quasi-cyclic LDPC block codes compares favorably with randomly generated LDPC codes for short to moderate lengths [7].

This paper has been discussed under the following sections. Section II is a brief description about PCM construction. Section III deals with the concept and working of LDPC. The algorithm for H matrix generation of Random LDPC and Quasi Cyclic LDPC are simulated and the simulation results are compared. The Hardware Implementation of generation of Random LDPC and both Quasi Cyclic LDPC is discussed in section IV. Section V covers the inferences drawn from the simulation as well as hardware implementation of both Random LDPC and Quasi Cyclic LDPC in terms of performance over AWGN channel.

II. PCM CONSTRUCTION

This section describes the random and structured quasi cyclic construction of PCM in terms of sparseness. The random matrix mostly ensembles block length, rank and rate. An algorithm is followed to fulfil the design requirements. A random H matrix with dimensions of rate 1/2 as in (324, 648) code, will have all rows to be linearly independent. Likewise matrix can be constructed for different rate and block length. If the rate is 2/5, the sparsity of random matrix is as shown in Fig 2.1

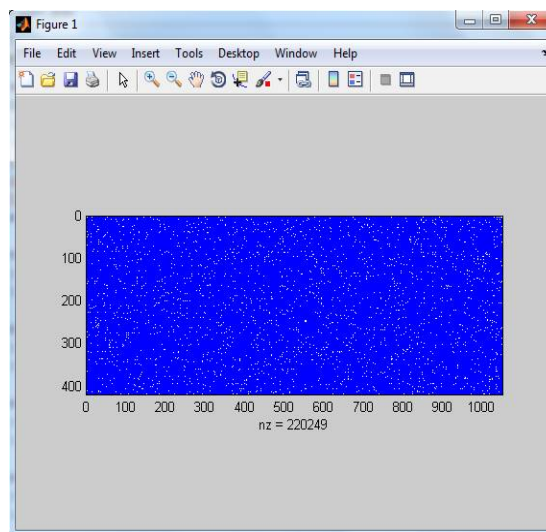


Fig 2.1 Sparse pattern for random matrix

The above Sparsity plot is obtained for randomly generated matrix for block length 1050. The matrix size is 525*1050. Number of non zero elements in randomly generated matrix is 220249. Density of matrix is defined as the ratio of number of non zero elements of the matrix to the total number of elements in the full matrix.

$$\text{Density of matrix} = \frac{\text{Number of non zero elements of the matrix}}{\text{Total number of elements in the full matrix}}$$

$$\text{Density of matrix} = 0.3$$

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The random matrix construction provides complexity in computation and takes more area. In order to overcome such difficulty, structured method of matrix construction was realized. They have control over the number of non zero elements, thereby complexity in both area and computation can be reduced.

Quasi cyclic block codes can be constructed using multiplicative groups in term of integers mod m to refer to the number of circulations of identity matrices that construct various H matrix with a variety of length and rates. The construction starts by choosing a prime number m (i.e. GF (2)), the element from 0 to m – 1 form a field under addition and multiplication (mod m). Thus the nonzero elements of this field represent a cyclic multiplicative group. ‘a’ and ‘b’ are chosen to be nonzero elements with order of K and J respectively. And then form the P matrix with dimensions of J × K with elements from GF(m) as the following:

$$P = \begin{bmatrix} 1 & a & a^2 & \dots & a^{K-1} \\ b & ab & a^2b & \dots & a^{K-1}b \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ b^{J-1} & ab^{J-1} & a^2b^{J-1} & \dots & a^{K-1}b^{J-1} \end{bmatrix}$$

Then a (Jm × Km) H matrix is constructed by having m × m identity matrices (Ix) inserted with their rows circularly shifted to the left by (x – 1) positions according to the values of P matrix as the follows:

- The number of circulations of identity matrices that construct various H matrix with a variety of length and rates.
- The construction starts by choosing a prime number m (i.e., GF (2)), the element from 0 to m – 1 form a field under addition and multiplication (mod m).
- Thus the nonzero elements of this field represent a cyclic multiplicative group.
- a and b are chosen to be nonzero elements with order of K and J respectively. And then form the P matrix with dimensions of J × K with elements from GF(m) as shown in the matrix below:

$$H = \begin{bmatrix} I & I_a & I_{a^2} & \dots & I_{a^{K-1}} \\ I_b & I_{ab} & I_{a^2b} & \dots & I_{a^{K-1}b} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ I_{b^{J-1}} & I_{ab^{J-1}} & I_{a^2b^{J-1}} & \dots & I_{a^{K-1}b^{J-1}} \end{bmatrix}$$

- The rate R of the constructed code is up to 1 – J/K due to the independence between some of resulting rows of H matrix.
- The number of '1's in columns and rows is J and K in sequence; this makes it a regular LDPC code.
- The construction also can be extended to use nonprime integers with some modifications to sustain the regularity of the H matrix.

The sparsity plot for Quasi cyclic block length 1050 is shown in fig 3. The matrix size is 525*1050. Number of non zero elements in Quasi cyclic constructed matrix is 2100. Density of matrix is defined as the ratio of number of non zero elements of the matrix to the total number of elements in the full matrix.

$$\begin{aligned} \text{Density of matrix} &= \frac{\text{Number of non zero elements of the matrix}}{\text{Total number of elements in the full matrix}} \\ &= 0.0038 \end{aligned}$$

By analysing the sparsity plots, we infer that the quasi cyclic matrix pattern has least density value, there by the Sparsity of non zero elements is wide spread and the number elements involved in computation reduces, there by complexity in hardware can be reduced.

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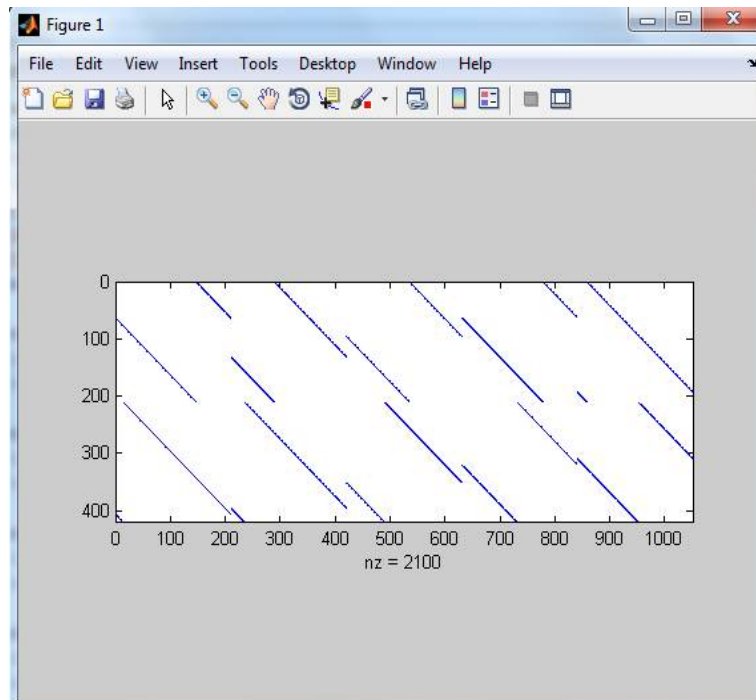


Fig. 2.2 Sparse pattern for quasi cyclic

III. SIMULATION RESULTS

The simulation has been performed using MATLAB R2013a. The LDPC code parameters and specifications used in the performance simulations are as follows:

- Code length 1050
- Matrix size 525×1050
- Rate 2/5
- SPA
- Column weight (w_c) of 3
- 10 iterations

The BER vs E_b/N_0 performance comparison curve between random and quasi cyclic codes are shown in Fig.3.1. Clearly quasi cyclic codes shows better BER performance when compared to random codes.

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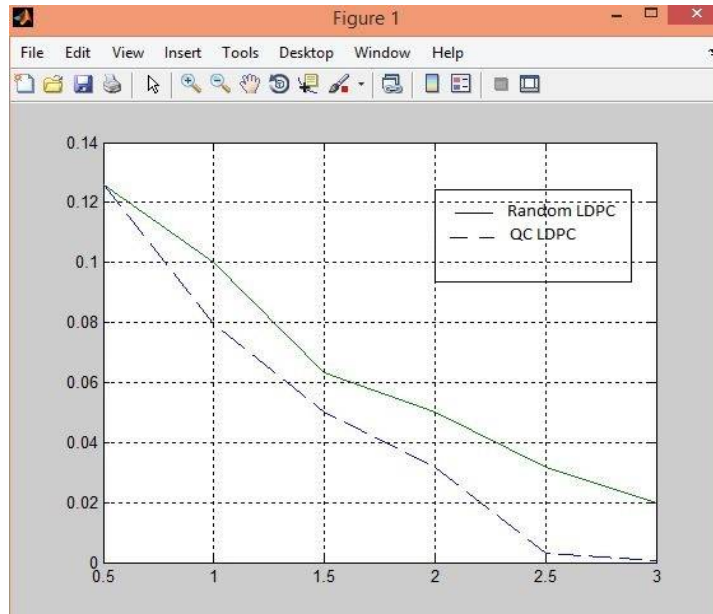


Fig. 3.1 Performance graph of random and quasi cyclic

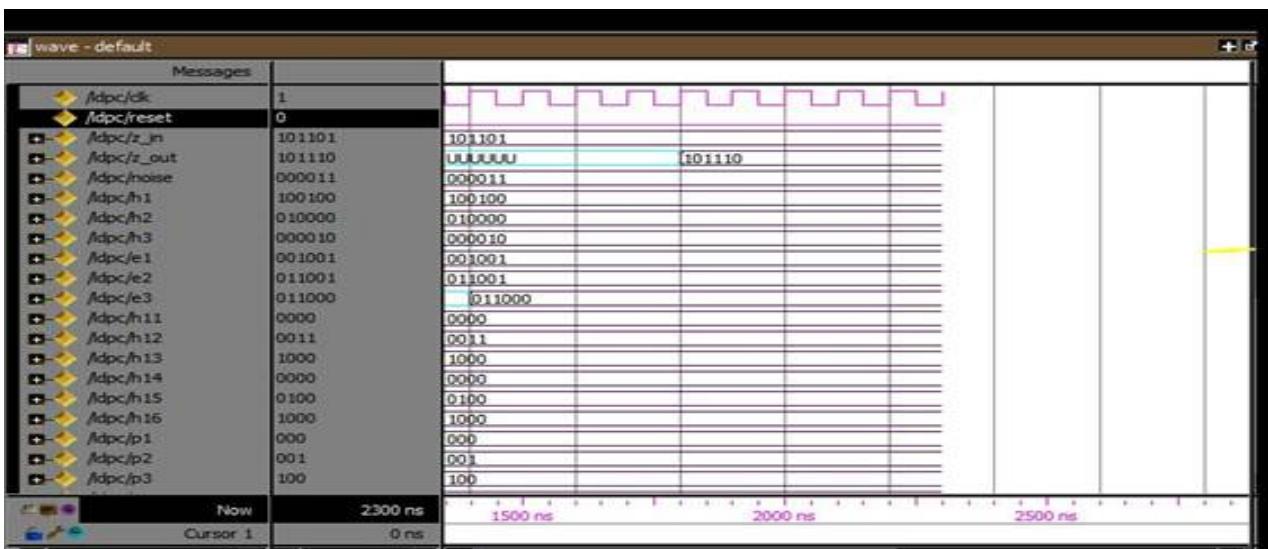


Fig. 3.2 Simulation of LDPC randomly generated codes

The above figure shows the randomly generated LDPC codes decoded with Sum Product Algorithm. Here 6 bits i.e. 101101 as shown are transmitted which forms H matrix by random fixation which are represented by h1, h2, h3 and this matrix is encoded which are represented as e1,e2,e3 and the received bits are decoded with Sum Product Algorithm with the parity p1,p2,p3. The decoded output 101110 where single bit is flipped.

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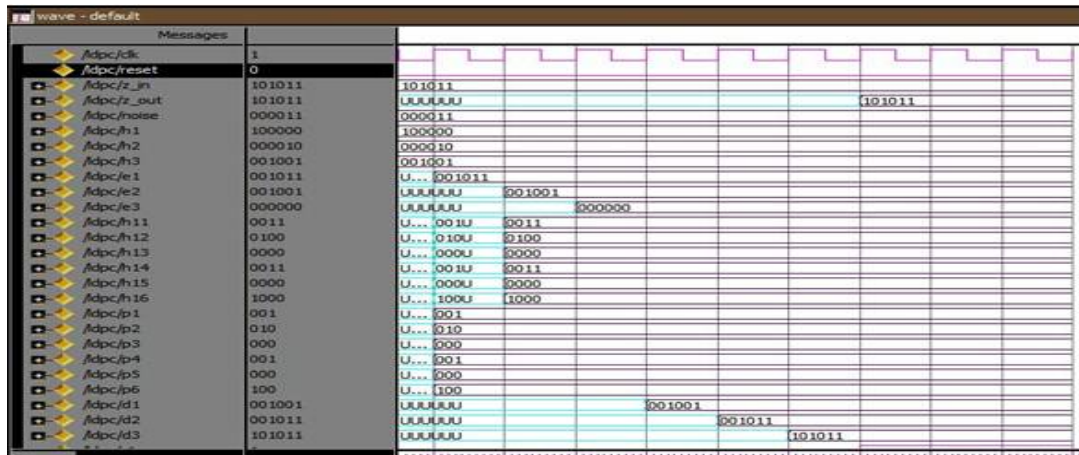


Fig 3.3 Simulation of LDPC Quasi Cyclic codes

This matrix is encoded which are represented as e1,e2,e3 and the received bits are decoded with Sum Product Algorithm with the parity p1,p2,p3 results in bits without any flipping ie 101011.

Fig 3.3 shows the Quasi Cyclic codes decoded with Sum Product Algorithm, where 6 bits i.e., 101011 as shown in are transmitted which forms H matrix by Quasi Cyclic fixation which are represented as h1,h2,h3.

IV. SYNTHESIS REPORT

The synthesis report for quasi cyclic and random codes is shown in table 4.1. The inference obtained from the synthesis report is that the constructed QC requires less number of registers, LUTs and FFs when compared to random LDPC codes. Hence the hardware complexity is nominal for QC.

LOGIC UTILIZATION	FOR QUASI CYCLIC CODES	FOR RANDOM CODES
Number of slice registers	22	30
Number of LUTs	15	19
Number of fully used LUT-FF pairs	14	18
Number of bonded IOBs	14	14

Table 4.1 : Comparison of performance metrics for Quasi Cyclic and Random codes

V HARDWARE IMPLEMENTATION

The binary inputs are given through UART to the reprogrammable FPGA. Two control switches are used to indicate two modes. Mode 1 is used for random LDPC codes. Mode 2 is used for Quasi cyclic LDPC codes. After the input is fed, it is decoded using Sum Product Algorithm and the result is viewed on the LCD display. The number of iterations can be increased in order to obtain error free output.

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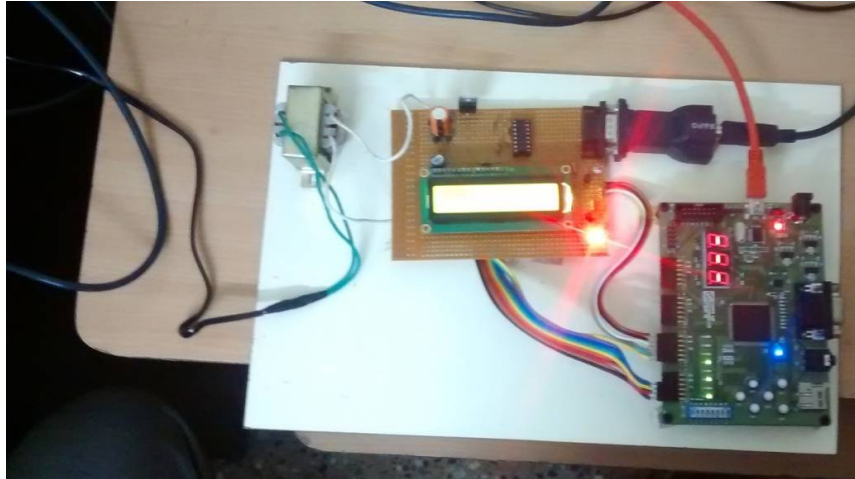


Fig 5.1 Experimental set up

VI. CONCLUSION

Binary QC LDPC has better decoding performance compared to random binary QC LDPC with block length 1050 of 2/5. The simulation results show that the constructed binary QC codes perform well over AWGN channel using Sum Product Algorithm Decoding. The proposed architecture for a (3, 6) code length is a framework model based on solely communicating the messages between the check node unit and the variable node unit. The architecture is designed for both random and Quasi cyclic codes with rate $\frac{1}{2}$. The designed logic is verified with the behavioural simulation and synthesized. The parameters like area are also evaluated with respect to the targeted Spartan device. The analysis can be extended for codes of higher order Galois field and high rate. Also further BER simulations at different lengths and rates will be necessary to evaluate the stability of performance of these codes.

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